Abstract of the Disclosure

An input buffered switch having a competing chance for transferring a cell at every time slot. The input buffered switches using pipelined simple matching, includes: a plurality of input unit for sending a request in every time slot in case that each Virtual Output Queue (VOQ) has at least one cell and outputting the cell according to a grant signal to each VOQ; a scheduling unit for executing a contention process according to requests from each VOQ of a plurality of input unit, sending contention results to a plurality of input unit and sending switch operating information to a switching unit; and the switching unit for switching and outputting the cell received from a plurality of input unit according to the switch operating information from the scheduling unit.